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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/422,539	10/21/1999	DING-KAI CHEN	10981786-1	5676

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EXAMINER	
KENDALL, CHUCK O	
ART UNIT	PAPER NUMBER
2122	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/422,539	Applicant(s) CHEN ET AL.	
	Examiner Chuck O Kendall	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10/21/1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This action is in response to the application filed 10/21/99

   Claims 1-16 have been examined.

2.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-16 are rejected under 35 U.S.C. 102(a) as being anticipated by Hayashi USPN 5,828,886.

CLAIM 1.

Hayashi anticipates a register usage indicator system for efficiently signaling register usage in a computer program comprising a plurality of blocks of code, said register usage indicator system comprising:[see Abstract register allotting and scheduling/availability]

a code usage register contained within a NOP instruction in one of the plurality of blocks of code in the computer program, said code usage register comprising a plurality of storage bits; and

[see 5:35-50 for bit vectors, see Fig 22 for NOP instructions and also see 25: 40-50 for NOP instructions and code usage register which is interpreted as the register information management and and scheduling feature from prior art by equivalent function]

a code register usage annotator for determining if each one of the plurality of registers is live in one of the plurality of blocks of code containing said NOP instruction.[see Fig 22,for NOP instruction, and live register within block of code, also]

CLAIM 2

The system of claim 1, wherein said code register usage annotator sets one of said plurality of storage bits in said code usage register for each one of the plurality of registers that is live in one of the plurality of blocks of code containing said NOP instruction.[see 25: 40-50 for register information management table and also refer back to 5: 40-45 for setting of bit vectors in the register information management table].

CLAIM 3

The system of claim 1, further comprising:

a register usage comparator for determining which of said registers are live in one of the plurality of blocks of code in the computer program by inspecting the bits set in said code usage register:[5:40-55,see register usage field and setting bit vectors]

contained in said NOP instruction.

[Also refer to 8:40-65,see table which shows a null set, which is also interpreted as a NOP instruction by definition, NULL operation or NO/NONE instruction operation (entry{none} gp1{sp ,ret, fp}) on line 43]

CLAIM 4

The system of claim 3, wherein said code register usage annotator determines whether or not each register is live in each one of the plurality of blocks of code containing said NOP instruction; and [5:40-55,see register usage field and setting bit vectors, see Kill or use as indicated by 1 or O for bit vectors in the register information management table as cited from prior art]

wherein said code register usage annotator sets each one of the plurality of storage bits in one of a plurality of storage code usage registers for each register live in each one of the plurality of blocks of code containing said NOP instruction.

[5:40-55, see register usage field and setting bit vectors, see Kill or use as indicated by 1 or O for bit vectors in the register information management table as cited from prior art]

CLAIM 5

The system of claim 4, wherein said register usage comparator determines which of said registers are not live in one of said plurality of blocks of code, by performing a logical OR of all of said plurality of storage code usage registers.

[12: 50-52, see whether or not bit vector is 1 being an indication for a live register, hence a 0 would be indicative of a not live register]

CLAIMs 6 &11

Hayashi anticipates a method to efficiently signal register usage in a computer program comprising a plurality of blocks of code, the method comprising the steps of: [Abstract and claims discloses both the method and the system as indicated in preamble]

determining which of a plurality of registers are live in one of the plurality of blocks of code in the computer program; [see Abstract for available registers, 4:20-25,see 5:35-50 for bit vectors and 25:40-50, for register information management table, and NOP instructions]

finding at least one NOP instruction in one of the plurality of blocks of code;[Fig 22]

creating a code usage register having a plurality of storage bits in said at least one NOP instruction in one of the plurality of blocks of code; and

[4:35-39, see renaming as interpreted from prior art, and refer back to 25:40-50 or NOP instructions]

setting one of said plurality of storage bits for each one of the plurality of registers live in one of the plurality of blocks of code containing said NOP instruction.

[see 5:35-50 for bit vectors and 12:50-52]

CLAIM 7&12

The method of claim 6, wherein said determining step further comprises the step of:

determining which of said plurality of registers are live in one of the plurality of blocks of code by inspecting the bits set in said code usage register.[5:42-48]

CLAIM 8

The method of claim 7, further comprising the step of:

determining which of the plurality of registers is live in each one of the plurality of blocks of code in the computer program.[5:60-65,see entire range of scheduling from register information management table]

CLAIM 9 & 15

The method of claim 8, further comprising the step of:

setting each one of said plurality of storage bits in one of a plurality of storage code usage registers for each register live in one of the plurality of blocks of code containing said NOP instruction.[5:35-50]

CLAIM 10 &16

Hayashi, anticipates the method of claim 9, further comprising the step of:

determining which of said registers are not live in all of the plurality of blocks of code, in the computer program, by performing a logical OR of all of said plurality of storage code usage. [12: 50-52, see whether or not bit vector is 1 being an indication for a live register, hence a 0 would be indicative of a not live register]

CLAIM 13

The system of claim 12, wherein said determining means further comprises:

means for inspecting the bits set in said code usage register to determine which of said registers are live in one of the plurality of blocks of code containing said NOP instruction.
[5:40-55, see register usage field and setting bit vectors, see Kill or use as indicated by 1 or O for bit vectors in the register information management table as cited from prior art]

CLAIM 14

The system of claim 13, further comprising:

means for determining which of the plurality of registers are live in each one of the plurality of blocks of code in the computer program.

[5:60-65, see entire range of scheduling from register information management table]

Correspondence Information

Any inquires concerning this communication or earlier communications from the examiner should be directed to Chuck O. Kendall who may be reached via telephone at (703) 308-6608. The examiner can normally be reached Monday through Friday between 8:00 A.M. and 5:00 P.M. est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Kevin Teska* may be reached at *(703) 305-9704.*

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is *(703) 305-3900.*

For facsimile (fax) send to 703-7467239 official and 703-7467240 draft

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PRIMARY EXAMINER